Form PTO-1449 Sheet 1 of 2
Applicant: Lewis B. Aronson et al. Confirmation No.:
Serial No.: 10/629,725 Att'y Docket No.: 15436.247.2.1.2
Filing Date: July 28, 2003 Group: 2661
For: INTEGRATED CIRCUIT WITH DUAL EYE OPENERS

INFORMATION DISCLOSURE CITATIONS MADE BY APPLICANT

U.S. Patent Documents

Examiner Initial*	Document Number	Issue Date	Name
EF 1	5,854,704	12/29/1998	Grandpierre
/l/ 2	6,256,127 B1	07/03/2001	Taylor
/l/ 3	4,932,038	06/05/1990	Windus
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/l/ 5	2002/0060824 A1	05/23/2002	Liou et al.
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Foreign Patent Documents

Examiner Initial*	Document Number	Publication Date	Country or Patent Office	Translation

Other Documents
(including author, title, pertinent pages, etc.)

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EF 7	*LXT16706/16707 SerDes Chipset,* Intel Products, www.intel.com/design/network/products/optical/phys/lxt16706.htm, April 19, 2002.
/l/ 8	*LXT35401 XAUI-to-Quad 3.2G Transceiver*, Intel Products, www.intel.com/design/network/products/optical/phys/lxt35401.htm, April 19, 2002.

Examiner: Date Considered: 10/3/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ac/b 9 Texas Instruments User's Guide, *TLK2201 Sedes EVM Kit Setup and Usage*, Mixed Signal DSP Solutions, July 2000.

/ 10 Texas Instruments User's Guide, *TLK1501 Serdes EVM Kit Setup and Usage*, Mixed Signal Products, June 2000.

/ 11 National Semiconductor DS92LV16 Design Guide, *Serializing Made Simple,* February 2002.

/ 12 Vaishali Semiconductor, *Fibre Channel Transceiver*, VN16117, MDSN-0002-02, 08/09/2001.

/ 13 Fairchild Semiconductor, Application Note 77, *CMOS, the Ideal Logic Family*, January 1983.

ac/b 14 Analog Target Specification, Annex 48B, Published by IEEE New York, 05/2001, pp. 6-14.

References Cited by Applicants

While the filing of Information Disclosure Statements is voluntary, the procedure is governed by the guidelines of Section 609 of the Manual of Patent Examining Procedure and 37 C.F.R. §§ 1.97 and 1.98. To be considered a proper Information Disclosure Statement, Form PTO-1449 shall be accompanied by a copy of each listed patent or publication or other item of information and a translation of the pertinent portions of foreign documents (if an existing translation is readily available to the applicant), an explanation of relevance of each reference not in the English language, and should be submitted in a timely manner as set out in MPEP Sec. 609.

Examiners will consider all citations submitted in conformance with 37 C.F.R. § 1.98 and MPEP Sec. 609 and place their initials adjacent the citations in the spaces provided on this form. Examiners will also initial citations not in conformance with the guidelines which may have been considered. A reference may be considered by the Examiner for any reason whether or not the citation is in full conformance with the guidelines. A line will be drawn through a citation if it is not in conformance with the guidelines AND has not been considered. A copy of the submitted form, as reviewed by the Examiner, will be returned to the applicant with the next communication. The original of the form will be entered into the application file.

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The reference designations "A1," "A2," etc. (referring to Applicant's reference 1, Applicant's reference 2, etc.) will be used by the Examiner in the same manner as Examiner's reference designations "A," "B," "C," etc. on Office Action Form PTO-1142.

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Examiner: Date Considered: 10/13/05

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